INTEGRATED CIRCUITS

DATA SHEET

TDA9845
TV and VTR stereo/dual sound processor with digital identification

Preliminary specification
Supersedes data of January 1993
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

FEATURES

- Supply voltage 5 to 8 V
- Source selector
- Stereo matrix
- AF input for mono source
- AF outputs for Main
- LED operation mode indication (stereo and dual)
- High identification reliability.

GENERAL DESCRIPTION

The TDA9845 is a stereo/dual sound processor for TV and VTR sets. Its identification ensures safe operation by using internal digital PLL technique with extremely small bandwidth, synchronous detection and digital integration (switching time maximum 2.1 s; identification concerning the main functions).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 18)		4.5	5	8.8	V
I_P	supply current (pin 18)	without LED current	12	13	16.5	mA
$V_{i(rms)}$	nominal input signal voltage ($V_{i\,1}$, $V_{i\,2}$, $V_{i\,3}$) (RMS value)	54% modulation				
		B/G	–	250	–	mV
		L (only for $V_{i\,1}$)	–	500	–	mV
$V_{o(rms)}$	nominal output signal voltage (RMS value)	54% modulation	–	500	–	mV
$V_{o(rms)}$	clipping level of the output signal voltages (RMS value)	THD ≤1.5%				
		V_P = 5 V	1.4	1.6	–	V
		V_P = 8 V	2.4	2.65	–	V
I_{LON}	input current	LED ON	–	–	12	mA
$V_{i\,pil}$	input voltage sensitivity of pilot frequency	unmodulated	5	–	100	mV
S/N(W)	weighted signal-to-noise ratio	*“CCIR468-3”*	66	75	–	dB
THD	total harmonic distortion		–	0.2	0.3	%
T_{amb}	operating ambient temperature range		0	–	+70	°C
f_{ident}	identification window width	STEREO	2.2	–	2.2	Hz
		DUAL	2.3	–	2.3	Hz
$t_{ident\,ON}$	total identification time ON		0.35	–	2.1	s
$V_{i\,tuner}$	identification voltage sensitivity		–	28	–	dBμV
Δf_{pil}	pull-in frequency range of pilot PLL	f_ω = 10.008 MHz				
		lower side	–296	–	–296	Hz
		upper side	302	–	302	Hz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9845	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA9845T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAMS

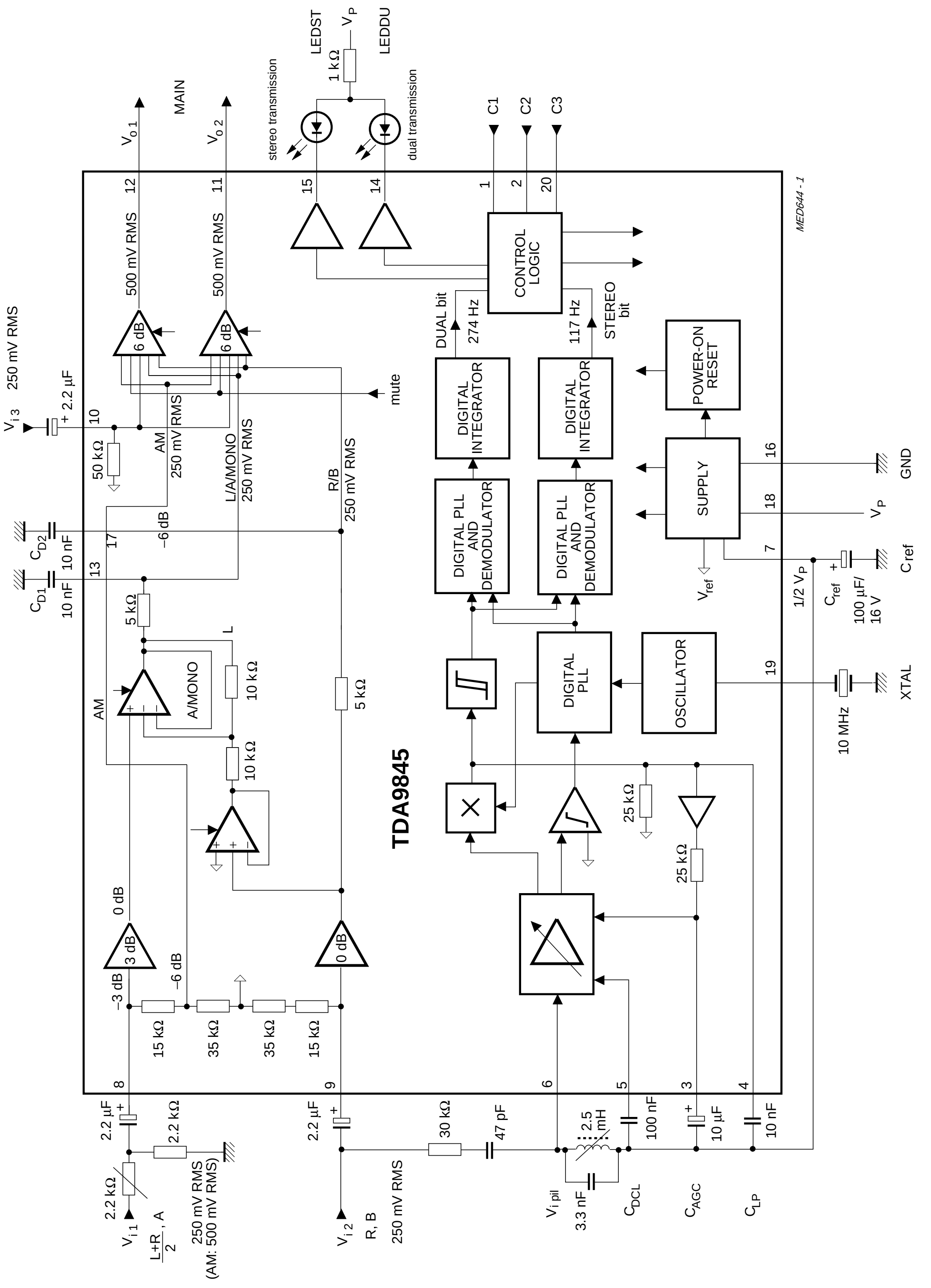
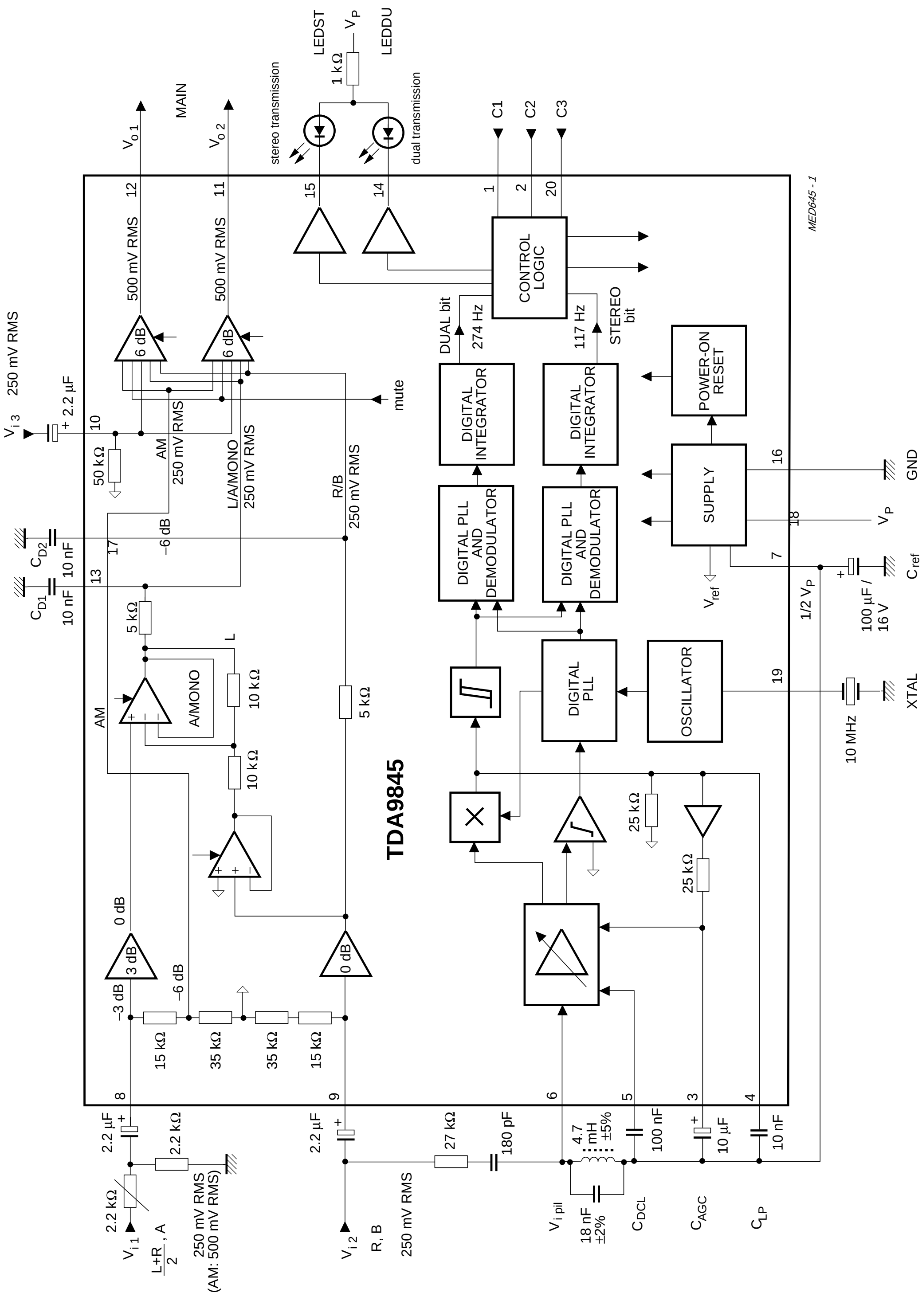


Fig.1 Block diagram of the bipolar TV/VTR-stereo decoder.

Input and output levels are nominal values.
They are related to the SCART norm.
(AM: m = 0.54, FM: Δf = ±27 kHz).



The components of the external LC band-pass filter have the following order-No.:
Philips Germany only No: 431202017525 or Fastron Sdn. Bha., Malaysia type
SMCC 472 J for L = 4.7 MHz (±5%)
Philips Components No: 2222 429 71802, C = 1.8 nF (±2%).

Input and output levels are nominal values.
They are related to the SCART norm.
(AM: m = 0.54, FM: Δf = ±27 kHz).

Fig.2 Block diagram of the bipolar TV/VTR-stereo decoder with fixed coil (alignment-free).

PINNING

SYMBOL	PIN	DESCRIPTION
C1	1	control input Port C1
C2	2	control input Port C2
C_{AGC}	3	AGC capacitor of pilot frequency amplifier
C_{LP}	4	identification low-pass capacitor
C_{DCL}	5	DC loop capacitor
$V_{i\ pil}$	6	pilot frequency input voltage
C_{ref}	7	capacitor of reference voltage ($\frac{1}{2}V_P$)
$V_{i\ 1}$	8	AF input signal voltage 1 (from sound carrier 1 or AM sound (standard L)
$V_{i\ 2}$	9	AF input signal voltage 2 (from sound carrier 2)
$V_{i\ 3}$	10	AF input signal voltage 3 (Mono sound)
$V_{o\ 2}$	11	AF output signal voltage 2 (Main)
$V_{o\ 1}$	12	AF output signal voltage 1 (Main)
C_{D1}	13	50 µs de-emphasis capacitor of AF Channel 1
LEDDU	14	LED (dual)
LEDST	15	LED (stereo)
GND	16	ground (0 V)
C_{D2}	17	50 µs de-emphasis capacitor of AF Channel 2
V_P	18	supply voltage (+5 to +8 V)
XTAL	19	10 MHz crystal input
C3	20	control input Port C3

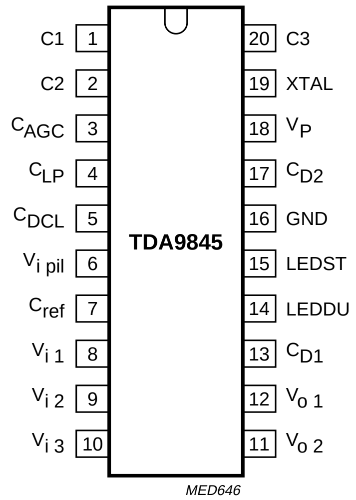


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

AF signal handling

The input AF signals, derived from the two sound carriers, are processed in analog form using operational amplifiers. Dematrixing uses the technique of two amplifiers processing the AF signals. Finally, a source selector provides the facility to route the mono signal through to the outputs (‘forced mono’).

De-emphasis is performed by two RC low-pass filter networks with internal resistors and external capacitors. This provides a frequency response with the tolerances given in Fig.4.

A source selector, controlled via the control input ports allows selection of the different modes of operation in accordance with the transmitted signal. The device was designed for a nominal input signal (FM: 54% modulation is equivalent to $\Delta f = \pm 27$ kHz) of 250 mV RMS ($V_{i\,1}$, $V_{i\,2}$) and for a nominal input signal (AM: m = 0.54) of 500 mV RMS ($V_{i\,1}$), respectively 250 mV RMS ($V_{i\,3}$). A nominal gain of 6 dB for $V_{i\,1}$ and $V_{i\,2}$ signals (0 dB for $V_{i\,1}$ signal (AM sound)) and 6 dB for $V_{i\,3}$ signal is built-in. By using rail-to-rail operational amplifiers, the clipping level (THD ≤1.5%) is 1.60 V RMS for V_P = 5 V and 2.65 V RMS for V_P = 8 V at outputs $V_{o\,1}$, $V_{o\,2}$. Care has been taken to minimize switching plops. Also total harmonic distortion and random noise are considerably reduced.

Identification

The pilot signal is fed via an external RC high-pass filter and single tuned LC band-pass filter to the input of a gain controlled amplifier. The external LC band-pass filter in combination with the external RC high-pass filter should have a loaded Q-factor of approximately 40 to 50 to ensure the highest identification sensitivity. By using a fixed coil (±5%) to save the alignment (see Fig.2), a Q-factor of approximately 12 is proposed. This may cause a loss in sensitivity of approximately 2 to 3 dB. A digital PLL circuit generates a reference carrier, which is synchronized with the pilot carrier. This reference carrier and the gain controlled pilot signal are fed to the AM-synchronous demodulator. The demodulator detects the identification signal, which is fed through a low-pass filter with external capacitor C_{LP} (pin 4) to a Schmitt-trigger for pulse shaping and suppression of low level spurious signal components. This is a measure against mis-identification.

The identification signal is amplified and fed through an AGC low-pass filter with external capacitor C_{AGC} (pin 3) to obtain the AGC voltage for controlling the gain of the pilot signal amplifier.

The identification stages consist of two digital PLL circuits with digital synchronous demodulation and digital integrators to generate the stereo or dual sound identification bits which can be indicated via LEDs.

A 10 MHz crystal oscillator provides the reference clock frequency. The corresponding detection bandwidth is larger than ±50 Hz for the pilot carrier signal, so that f_p-variations from the transmitter can be tracked in the event of missing synchronization with the horizontal frequency f_H. However the detection bandwidth for the identification signal is made small (±1 Hz) to reduce mis-identification.

Figure 2 shows an example of the alignment-free f_p band-pass filter. To achieve the required Q_L of around 12, the Q_0 at f_p of the coil was chosen to be around 25 (effective Q_0 including PCB influence). Using coils with other Q_0, the RC-network (R_{FP}, C_{FP}) has to be adapted accordingly. It is assumed that the loss factor $\tan\delta$ of the resonance capacitor is ≤0.01 at f_p.

Copper areas under the coil might influence the loaded Q and have to be taken into account. Care has also to be taken in environments with strong magnetic fields when using coils without magnetic shielding.

Control input ports

The complete IC is controlled by the three control input ports C1, C2 and C3 (TTL-level). With these ports the user can select between different AF sources according to the transmitter status (see Table 1). Finally Schmitt-triggers are added in the input port interfaces to suppress spikes from the control lines C1, C2 and C3.

After a power-on reset, the logic is reset (mute mode for the AF channel). After some time (≤1 ms), when the power-on reset is automatically deactivated, the switch position of the Main channel is changed according to the control input port levels C1, C2 and C3.

For standard L, the AM sound is fed via the AF input ($V_{i\,1}$) to the two AF outputs ($V_{o\,1}$,$V_{o\,2}$). This can also be achieved by feeding at AF input $V_{i\,3}$.

The logic level combination 111 of the control input ports (C3, C2 and C1) is **not allowed** (see Table 1).

Power supply

The different supply voltages and currents required for the analog and digital circuits are derived from an internal band-gap reference circuit. The AF reference voltage is $\frac{1}{2}V_P$. For a fast setting to $\frac{1}{2}V_P$ an internal start-up circuit is added. A good ripple rejection is achieved with the external capacitor C_{ref} = 100 μF/16 V in conjunction with the high ohmic input of the $\frac{1}{2}V_P$ pin (pin 7). No additional DC load on this pin is allowed.

Power-on reset

When a power-on reset is activated by switching on the supply voltage or because of a supply voltage breakdown, the 117/274 Hz DPLL, the 117/274 Hz integrator and the logic will be reset. The AF channel (Main) is muted (≤1 ms).

ESD protection

All pins are ESD protected. The protection circuits represent the latest state of the art.

Internal circuit

The internal pin loading diagram is given in Fig.7.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)		–0.3	10	V
V_i	voltage at pins 1, 2 and 20		–0.3	9.0	V
V_i	voltage at pins 3 to 13, 17 and 19		–0.3	V_P	V
V_i	voltage at pins 14 and 15		–0.3	10	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_{esd}	electrostatic handling for all pins	note 1	–500	+500	V

Note

1. Charge device model class A: discharging a 200 pF capacitor through a Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIP20	73	K/W
	SO20	90	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = +25 °C; nominal input signal $V_{i\,1,\,2}$ = 0.25 V RMS value (FM: 54% modulation is equivalent to Δf = ±27 kHz); nominal input signal $V_{i\,1}$ = 0.5 V RMS value (AM: m = 0.54); nominal input signal $V_{i\,3}$ = 0.25 V RMS value (AM: m = 0.54); nominal output signal $V_{o\,1,\,2}$ = 0.5 V RMS value; f_{AF} = 1 kHz; $V_{i\,pil}$ = 16 mV RMS value; f_{pil} = 54.6875 kHz (identification frequencies: stereo = 117.48 Hz, dual = 274.12 Hz), 50 µs pre-emphasis; noise measurement in accordance with *"CCIR468-3"*, working oscillator frequency f_{ω} = 10008 MHz; currents into the IC positive; measured in test circuit Fig.5 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 18)		4.5	5	8.8	V
I_P	supply current (pin 18)	without LED current	12	13	16.5	mA
P_{tot}	total power dissipation		54	65	145.2	mW
$V_{n(DC)}$	DC voltage (pins 8 to 13 and 17)		$\frac{1}{2}V_P - 0.1$	$\frac{1}{2}V_P$	$\frac{1}{2}V_P + 0.1$	V
$V_{ref(DC)}$	DC reference voltage (pin 7)		$\frac{1}{2}V_P - 0.1$	$\frac{1}{2}V_P$	$\frac{1}{2}V_P + 0.1$	V
$I_{L(DC)}$	DC leakage current (pin 7)		–	–	±1	µA
AF Inputs; $V_{i\,1}$ and $V_{i\,2}$ (pins 8 and 9)						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation				
		B/G	–	0.25	–	V
		L (only $V_{i\,1}$)	–	0.5	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V; B/G	0.625	0.715	–	V
		V_P = 8 V; B/G	1.050	1.200	–	V
		V_P = 5 V; L (only $V_{i\,1}$)	1.200	1.600	–	V
		V_P = 8 V; L (only $V_{i\,1}$)	2.100	2.356	–	V
G_v	AF signal voltage gain	$G = V_o/V_i$; note 1				
		B/G	5	6	7	dB
		L (only $V_{i\,1}$)	–1	0	+1	dB
R_i	input resistance		40	50	60	kΩ
R_{deem}	internal de-emphasis resistor (pins 13 and 17)	see Fig.4	4.25	5.0	5.75	kΩ
Additional AF input pin (pin 10)						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation	–	0.25	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	0.625	0.715	–	V
		V_P = 8 V	1.050	1.200		V
G_v	AF signal voltage gain	$G = V_o/V_i$; note 1	5	6	7	dB
R_i	input resistance		40	50	60	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AF outputs (pins 11 and 12)						
$V_{o(rms)}$	nominal output signal voltage (RMS value)	THD ≤ 0.3%; 54% modulation	–	0.5	–	V
$V_{o(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	1.4	1.6	–	V
		V_P = 8 V	2.4	2.65	–	V
R_o	output resistance		150	250	350	Ω
C_L	load capacitor on output		–	–	1.5	nF
R_L	load resistor on output (AC-coupled)		10	–	–	kΩ
B	frequency response (bandwidth)	f_i = 40 to 20000 Hz; note 2	–0.5	–	+0.5	dB
$B_{-3\ dB}$	frequency response	–3 dB; note 2	300	350	400	kHz
THD	total harmonic distortion	note 1	–	0.2	0.3	%
S/N(W)	weighted signal-to-noise ratio	*“CCIR468-3”* (quasi-peak)	66	75	–	dB
α_{cr}	crosstalk attenuation for	notes 1 and 3				
	DUAL	$\lvert Z_S \rvert$ ≤ 1 kΩ	70	75	–	dB
	STEREO	$\lvert Z_S \rvert$ ≤ 1 kΩ	40	45	–	dB
α_{mute}	mute attenuation	$\lvert Z_S \rvert$ ≤ 1 kΩ; note 1	76	80	–	dB
ΔV_{DC}	change of DC level output voltage between any two modes of operation	after switching	–	–	±10	mV
PSRR	power supply ripple rejection	f_r = 70 Hz; see Fig.6	50	65	–	dB
$I_{O(DC)}$	DC output current		–	–	±20	µA
10 MHz crystal oscillator (pin 19)						
f_r	series resonant frequency of crystal (fundamental mode)	C_L = 20 pF	9.995	10.008	10.021	MHz
f_ω	working oscillator frequency (running in parallel resonance mode)	over operating temperature range including ageing and influence of drive circuit	9.988	10.008	10.028	MHz
R_r	equivalent crystal series resistance	even at extremely low drive level (<1 pW) over operating temperature range with C_0 = 6 pF	–	60	200	Ω
R_n	crystal series resistance of unwanted mode		2 × R_r	–	–	Ω
C_0	crystal parallel capacitance	with R_r ≤ 100 Ω	–	6	10	pF
C_1	crystal motional capacitance		–	25	50	fF
P_{XTAL}	level of drive in operation		–	–	5	µW
$V_{OSC(p-p)}$	oscillator operating voltage (peak-to-peak value)		500	550	600	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pilot processing						
$V_{i\ pil(rms)}$	pilot input voltage level at pin 6 (RMS value)	unmodulated	5	–	100	mV
$R_{i\ pil}$	pilot input resistance		500	1000	–	kΩ
$C_{i\ pil}$	pilot input capacitance		–	–	3	pF
m	modulation depth	AM	25	50	75	%
Δf_{pil}	pilot PLL pull-in frequency range (referenced to f_{pil} = 54.6875 kHz)	f_{ω} = 9.988 MHz				
		lower side	–405	–	–405	Hz
		upper side	192	–	192	Hz
		f_{ω} = 10.008 MHz				
		lower side	–296	–	–296	Hz
		upper side	302	–	302	Hz
		f_{ω} = 10.028 MHz				
		lower side	–188	–	–188	Hz
		upper side	411	–	411	Hz
t_{pil}	pilot PLL pull-in time		0	–	1.7	ms
f_{LP}	low-pass frequency response	–3 dB	450	600	750	Hz
R_4	low-pass output resistance		18.75	25	31.25	kΩ
$V_{4(rms)}$	identification threshold voltage (RMS value)		–	–	70	mV
Q_L	loaded quality factor of resonance circuit	HIGH sensitivity; see Fig.1	40	–	50	
	loaded quality factor of resonance circuit with fixed coil	sensitivity loss 2 to 3 dB; see Fig.2	–	12	–	
$t_{acqui\ AGC}$	AGC acquisition time	$V_{i\ pil(rms)}$ switched from 0 to 100 mV RMS value	–	–	0.1	s
Identification (internal functions)						
$V_{i\ tuner}$	identification voltage sensitivity	note 4	–	28	–	dBμV
C/N	pilot carrier-to-noise ratio for start of identification	note 5	–	33	–	dB/Hz
H	hysteresis	note 4	–	–	2	dB
f_{det}	pull-in frequency range of identification PLL (referenced to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	lower side				
		STEREO	–0.63	–	–0.63	Hz
		DUAL	–0.69	–	–0.69	Hz
		upper side				
		STEREO	0.63	–	0.63	Hz
		DUAL	0.69	–	0.69	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{det}	pull-in time of identification PLL (referenced to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	STEREO	0	–	0.8	s
		DUAL	0	–	0.8	s
f_{ident}	identification window frequency width (referenced to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	STEREO; note 6	2.2	–	2.2	Hz
		DUAL; note 6	2.3	–	2.3	Hz
t_{integr}	integrator time constant		0.94	–	0.94	s
$t_{ident(on)}$	total identification time on	STEREO; note 7	0.35	–	2.0	s
		DUAL; note 7	0.35	–	2.0	s
$t_{ident(off)}$	total identification time off	STEREO; note 8	0.60	–	1.5	s
		DUAL; note 8	0.60	–	1.5	s
LED (pins 14 and 15)						
$V_{L(off)}$	output voltage	LED off	–	–	8.8	V
$V_{L(on)}$	output voltage	LED on	–	–	0.7	V
$I_{L(off)}$	input current	LED off	–	–	1	μA
$I_{L(on)}$	input current	LED on	–	–	12	mA
Control input ports C1, C2 and C3 (pins 1, 2 and 20)						
V_{CL}	LOW level input voltage		0	–	0.8	V
V_{CH}	HIGH level input voltage		2.4	–	8.8	V
I_{CL}	LOW level input current		–	–	–1	μA
I_{CH}	HIGH level input current		–	–	1	μA

Notes

1. V_o = 0.5 V RMS value; f = 1 kHz.
2. Without de-emphasis capacitors with respect to nominal gain.
3. In dual mode: A (B)-signal into B (A) channel.
   In stereo mode: R-signal into left channel; L-signal = 0.
4. Tuner input signal, measured with PCALH reference front end ($\frac{1}{2}$EMF, 75 Ω, 2T/20T/white bar, 100% video) and PC/SC_1 = 13 dB; PC/SC_2 = 20 dB. The pilot band-pass has to be aligned.
5. Bandwidth of the pilot BP-filter $B_{-3\ dB}$ = 1.2 kHz. $V_{i\ 2}$ input driven with identification-modulated pilot carrier and white noise.
6. Identification window is defined as twice the pull-in frequency range (lower plus upper side) of identification PLL (steady detection) plus window increase due to integrator (fluctuating detection).
7. The maximum total system identification time ON is equal to $t_{ident(on)}$ plus $t_{acqui\ AGC}$.
8. The maximum total system identification time OFF is equal to $t_{ident(off)}$.

Table 1 Control input port matrix to select AF inputs and AF outputs

INPUT/OUTPUT	MODE	INPUT SIGNAL			OUTPUT SIGNAL		CONTROL INPUT			LED	
		ST/DS/M		EXT	MAIN		PORT[1]				
		$V_{i\,1}$ PIN 8	$V_{i\,2}$ PIN 9	$V_{i\,3}$ PIN 10	$V_{o\,1}$ PIN 12	$V_{o\,2}$ PIN 11	C3 PIN 20	C2 PIN 2	C1 PIN 1	DUAL PIN 14	STEREO PIN 15
Mute; note 2	–	–	–	–	no signal		0	0	0	OFF	OFF
Sound mute	–	–	–	–	no signal		1	0	0	note 3	note 3
Mono	M	M	–	–	M	M	0	0	1	OFF	OFF
		M	–	–	M	M	0	1	0	OFF	OFF
		AM	–	–	AM	AM	0	1	1	OFF	OFF
Stereo	ST	S	R	–	L	R	0	0	1	OFF	ON
		S	R	–	S	S	0	1	0	OFF	ON
		S	R	–	S	S	0	1	1	OFF	ON
Dual	DS	A	B	–	A	B	0	0	1	ON	OFF
		A	B	–	A	A	0	1	0	ON	OFF
		A	B	–	B	B	0	1	1	ON	OFF
External; note 4	–	–	–	C	C	C	1	0	1	note 3	note 3
		–	–	C	C	C	1	1	0	OFF	OFF

Notes

1. The combination 111 is **not allowed**.
2. In mute mode the content of the 117 Hz/274 Hz integrator will be reset. The LEDs are switched OFF.
3. The LED show the identification status.
4. In external mode, in the combination 110 only the LEDs are switched OFF.

Table 2 Explanation of Table 1

SIGNAL	DESCRIPTION
R	right
L	left
S	$\frac{(L+R)}{2}$
A and B	dual sound A/B
C	external sound source
AM	AM sound (standard L)
M	mono sound
DS	dual sound
ST	stereo sound

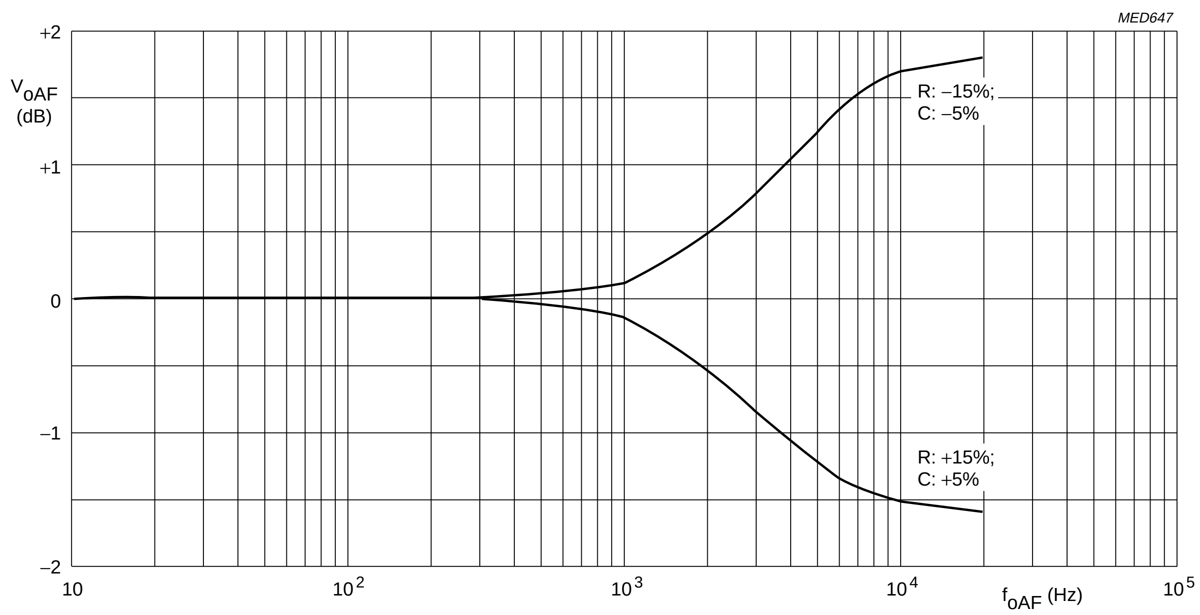


Fig.4 Tolerance scheme of AF frequency response; de-emphasis with C_{D1}, C_{D2} = 10 nF (±5%), $R_{internal}$ = 5 kΩ (±15%).

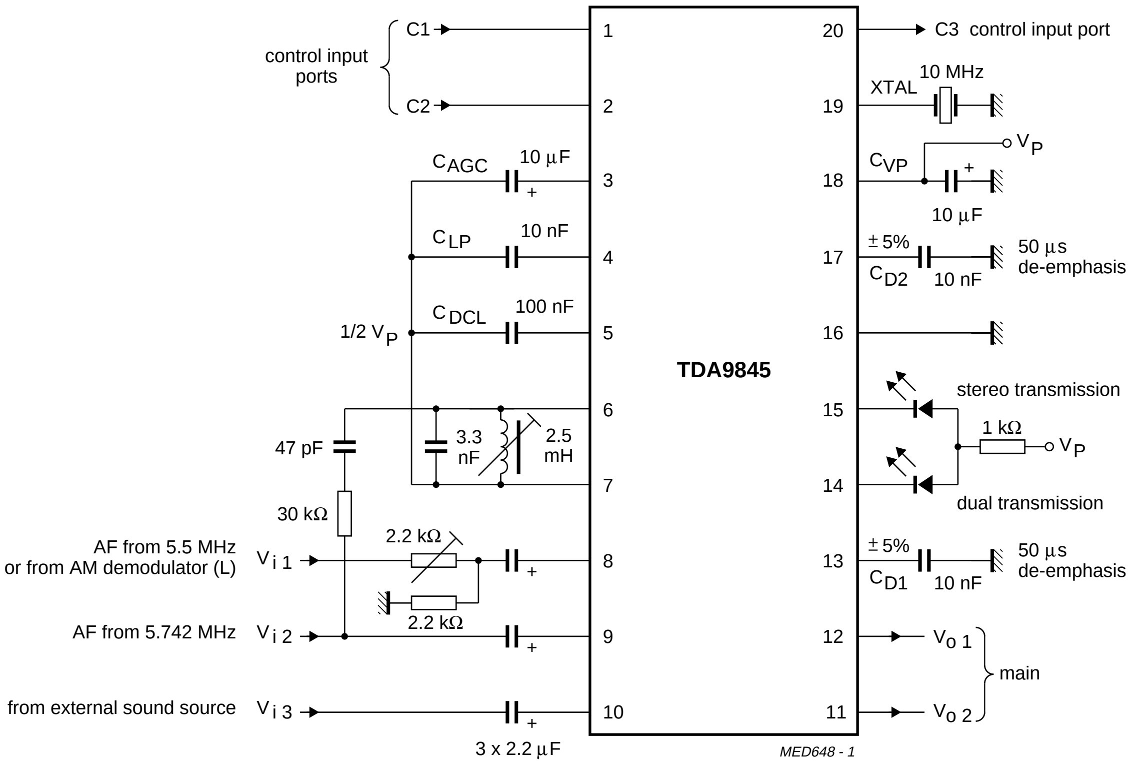


Fig.5 Test circuit of the stereo decoder TDA9845.

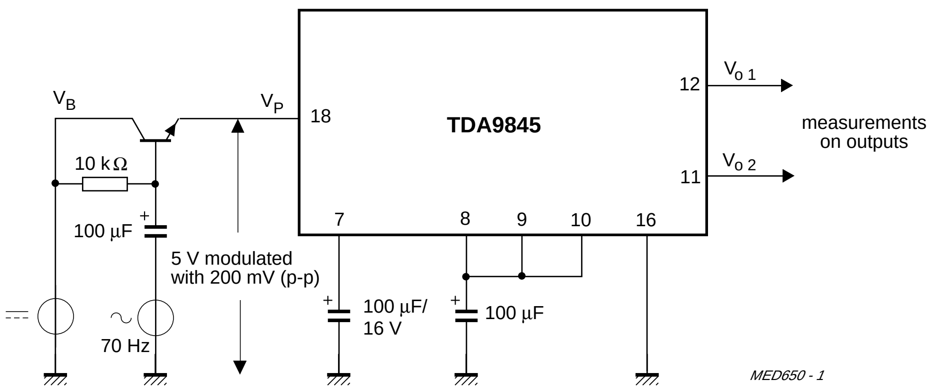


Fig.6 Test circuit for measurement of ripple rejection.

INTERNAL CIRCUITRY

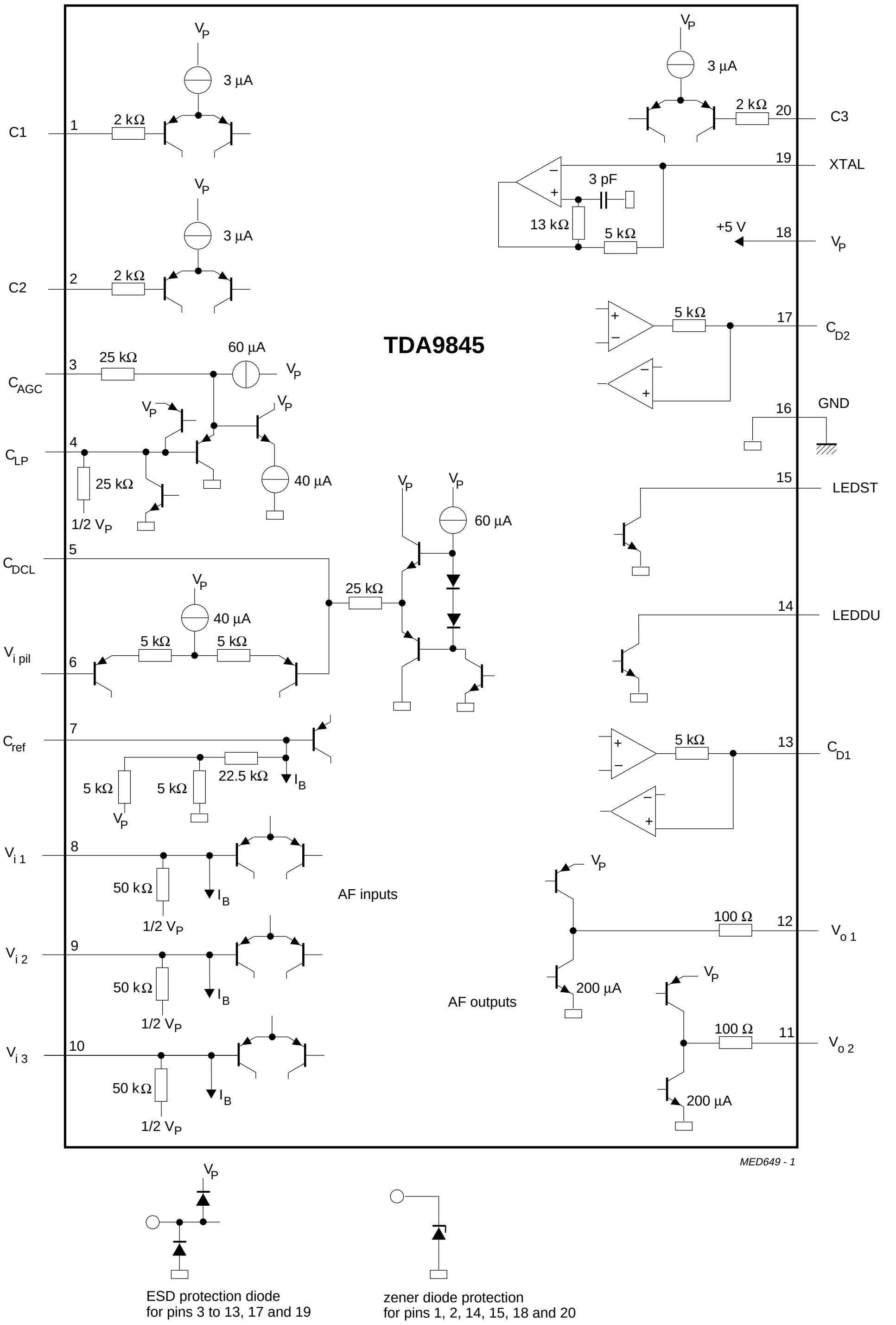
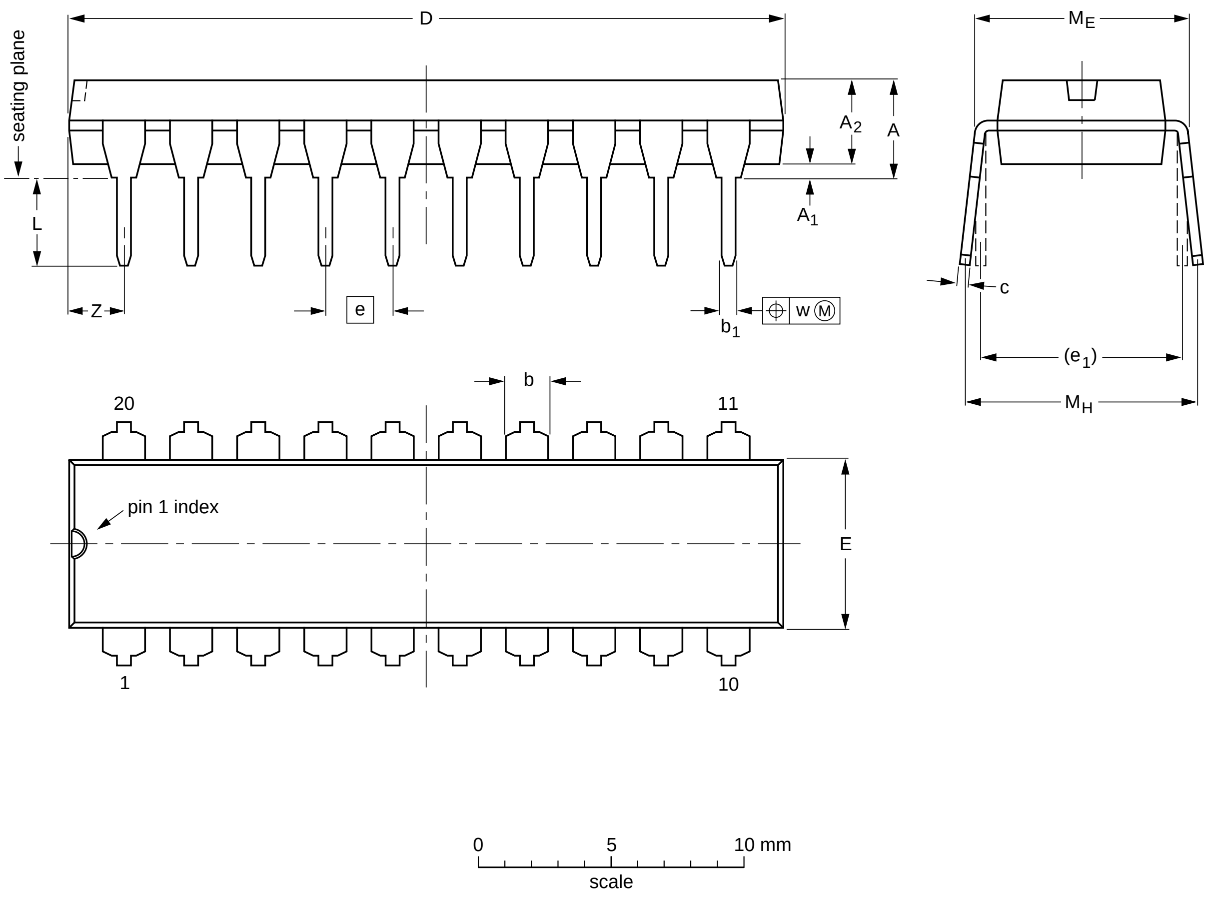


Fig.7 Internal circuitry.

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

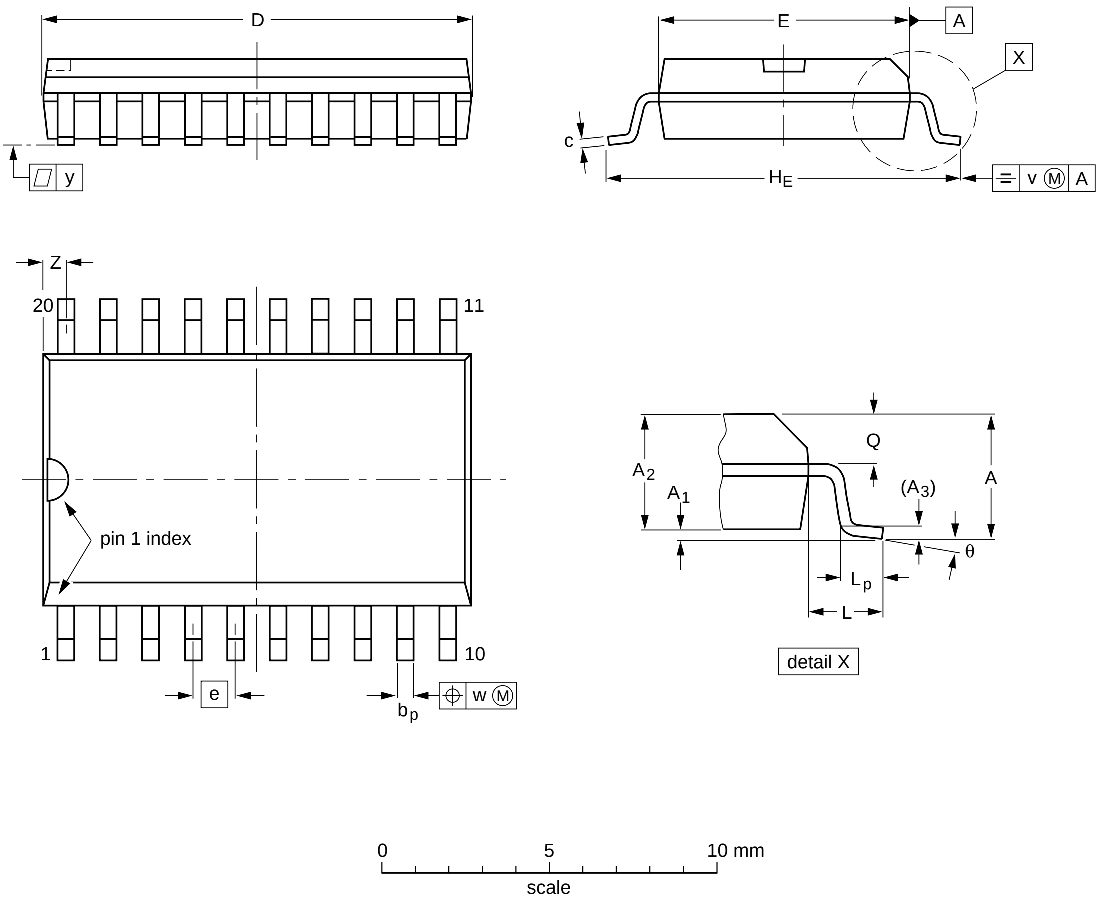
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON 4OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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